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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,839	12/27/2001	Christopher L. Hamlin	01-827	9625

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EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,839	HAMLIN, CHRISTOPHER L.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,5,7,11,12,14,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,7,11,14 and 18* is/are rejected.

7)☒ Claim(s) *3,12 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 May 2004 has been entered.

2. Applicant's amendment to 10/034,839 has been examined. Claims 1, 4, 6, 8-10, 13, 15-17, and 20 are cancelled. Claims 2, 3, 5, 7, 11, 12, 14, 18, and 19 are pending.

3. After further consideration, the indication of allowability of claims 2, 3, 5, 7, 11, 12, 14, 18, and 19 based on new grounds of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Pursuant to claim 5, the limitation "the training of a neural network" not only lacks antecedent basis but also it is unclear how this limitation of a "neural network" relates to the rest of the claimed limitations such as platform architecture and support methodology. Inotherwords, there is a structural/functional gap

between the "training of a neural network" and the rest of the claim. Furthermore, the specification doe not elaborate on the meaning of a neural network.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Rejection of claims 2, 5, 7, 11, 14 and 18

6. Claims 2, 5, 7, 11, 14, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Koza et al. (Koza), U.S. Patent 5,742,738. Koza discloses the simultaneous evolution of the architecture of a multi-part program to solve a problem using architecture altering operations.

7. Pursuant to claim 2, which recites a system suitable for providing integrated circuit design (col. 1, ll. 24-28), comprising a memory storing a first set of instructions, and a processor communicatively coupled to the memory, the processor suitable for performing the first set of instructions and the second set of instructions, wherein the first set of instructions is suitable for configuring a processor to provide an integrated circuit development environment in which a support methodology for an integrated circuit is created and the second set of instructions is suitable for configuring a processor to provide tools for implementing a platform architecture of an integrated circuit (col. 5, ll. 44-67) in which the platform architecture supplies a structure of the integrated circuit, (col. 4, ll. 21-53) the first set of instructions and the second set of

instructions linked through at least one formalism so that at least one of an action taken utilizing the platform architecture influences the support methodology and an action taken utilizing the support methodology influences the platform architecture; wherein the formalism includes a differential game (col. 5, ll. 44-67).

8. Pursuant to claim 5, which recites a system suitable for providing integrated circuit design (col. 1, ll. 24-28), comprising a memory storing a first set of instructions, and a processor communicatively coupled to the memory, the processor suitable for performing the first set of instructions and the second set of instructions, wherein the first set of instructions is suitable for configuring a processor to provide an integrated circuit development environment in which a support methodology for an integrated circuit is created and the second set of instructions is suitable for configuring a processor to provide tools for implementing a platform architecture of an integrated circuit (col. 5, ll. 44-67) in which the platform architecture supplies a structure of the integrated circuit, (col. 4, ll. 21-53) the first set of instructions and the second set of instructions linked through at least one formalism so that at least one of an action taken utilizing the platform architecture influences the support methodology and an action taken utilizing the support methodology influences the platform architecture; wherein the formalism includes a genetic algorithm (col. 10, ll. 44-62); and wherein the genetic algorithm guides the training of a neural network (col. 11, ll. 4-62).

9. Pursuant to claim 7, which recites a system suitable for providing integrated circuit design (col. 1, ll. 24-28), comprising a memory storing a first set of instructions, and a processor communicatively coupled to the memory, the processor suitable for

performing the first set of instructions and the second set of instructions, wherein the first set of instructions is suitable for configuring a processor to provide an integrated circuit development environment in which a support methodology for an integrated circuit is created and the second set of instructions is suitable for configuring a processor to provide tools for implementing a platform architecture of an integrated circuit (col. 5, ll. 44-67) in which the platform architecture supplies a structure of the integrated circuit, (col. 4, ll. 21-53) the first set of instructions and the second set of instructions linked through at least one formalism so that at least one of an action taken utilizing the platform architecture influences the support methodology and an action taken utilizing the support methodology influences the platform architecture; wherein the formalism is utilized to implement a coevolutionary relationship (col. 10, ll. 44-59); and wherein the coevolutionary relationship is implemented between the platform architecture and the support methodology (col. 10, ll. 44-59).

10. Pursuant to claim 11, which recites a method of designing an integrated circuit, comprising: receiving functional specifications and constraints of an integrated circuit (col. 5, ll. 36-53), and interacting with a system configured to provide an environment for deriving a support methodology for an integrated circuit having the received functional specifications, wherein the interaction with the support methodology for the integrated circuit influences an environment for designing a platform architecture for the integrated circuit, wherein the support methodology influences the environment for designing the platform architecture through the use of a formalism including a differential game (col. 5, ll. 44-67).

11. Pursuant to claim 14, which recites a method of designing an integrated circuit, comprising: receiving functional specifications and constraints of an integrated circuit (col. 5, ll. 36-53), and interacting with a system configured to provide an environment for deriving a support methodology for an integrated circuit having the received functional specifications, wherein the interaction with the support methodology for the integrated circuit influences an environment for designing a platform architecture for the integrated circuit, wherein the support methodology influences the environment for designing the platform architecture through the use of a formalism wherein the formalism is utilized to implement a coevolutionary relationship (col. 5, ll. 44-67), and wherein the coevolutionary relationship is implemented between the platform architecture and the support methodology (col. 10, ll. 44-59).

12. Pursuant to claim 18, which recites a method of designing an integrated circuit, comprising: receiving functional specifications and constraints of an integrated circuit (col. 5, ll. 36-53), and interacting with a system configured to provide an environment for deriving a platform architecture (col. 5, ll. 44-67) for an integrated circuit having the received functional specifications, wherein the interaction with the platform architecture for the integrated circuit influences an environment for designing a support methodology for the integrated circuit, wherein the platform architecture influences the environment for designing the support methodology through the use of a formalism including a differential game (col. 5, ll. 44-67),

Allowable Subject Matter

13. Claims 3, 12, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach the limitation wherein the formalism includes a zero sum differential game.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing.

16. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

17. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

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